# DIGITAL ELECTRONICS AND LOGIC DESIGN

*Unit III — Sequential Circuits, Counters & Finite State Machines*

---

**Topics Covered in this Unit**

Sequential Logic Foundations: Latches vs. Edge-Triggered Flip-Flops (Clock Skew, Setup & Hold Times)
Flip-Flop Architectures: SR, JK (Race-Around Condition & Master-Slave JK Solution), D (Data), and T (Toggle)
Comprehensive Truth Tables, Characteristic Equations & Excitation Tables for All Flip-Flops
Systematic Flip-Flop Conversion Methodology (Target Table → Excitation Mapping → K-Map Synthesis)
Shift Registers: SISO, SIPO, PISO, PIPO, Bidirectional & 4-Bit Universal Shift Register (IC 74194)
Shift Register Counters: Self-Starting Ring Counter (Mod-N) & Johnson / Twisted-Ring Counter (Mod-2N)
Asynchronous (Ripple) vs. Synchronous Binary Counters & Up/Down Counter Design
BCD Decade Counters: Architecture & Modulus Configuration of IC 7490 (MOD-10, MOD-6, MOD-60)
Synchronous Sequential Circuit Design: Mealy Machines vs. Moore Machines Architecture
State Reduction (Row Matching & Implication Table Methods) and State Assignment Techniques
High-Yield University Exam Question Bank with Detailed Model Answers & Unit Summary

*Compiled in a structured, easy-to-understand, textbook style format*
*Specially curated for B.Tech / B.E. / BCA / MCA / B.Sc Electronics, Electrical, CS & AI Students*

**© Copyright — abhyasmitra.in — All Rights Reserved**

# COURSE SYLLABUS & MAPPING

**[ UNIT III SYLLABUS — PRESCRIBED UNIVERSITY CURRICULUM ]**

*This section contains the official syllabus for Unit III. Verify with your university curriculum mapping.*

**Unit III Syllabus Breakdown:**

Unit III Sequential Circuits: Flip-Flop: SR, JK, D,T, MSJK, Truth Tables and Excitation tables, Conversion of Flip-Flop ,Shift Registers, Bidirectional Shift Register, Universal Shift Register, Ring Counter ,Johnson Counter Counters: Asynchronous Counter, Synchronous Counter, BCD Counter, Modulus of the counter ( IC 7490), Presettable Counter, Synchronous sequential circuits : Moore Circuit, Mealy Circuit, State Diagram, State table, State Reduction ,State Assignment

• Course Code: _____ • Semester / Year: _____

# TABLE OF CONTENTS

3.1 Flip-Flops: Types, Truth Tables & Excitation Tables ..... 1
Race-Around Condition & Master-Slave JK Flip-Flop ..... 1
3.2 Systematic Flip-Flop Conversion Methodology ..... 1
3.3 Shift Registers & Shift Register Counters ..... 1
1. Shift Register Configurations ..... 1
2. Ring Counter vs. Johnson Counter ..... 1
3.4 Counters: Asynchronous, Synchronous & IC 7490 ..... 1
Asynchronous (Ripple) vs. Synchronous Counters ..... 1
The IC 7490 BCD Decade Counter ..... 1
3.5 Synchronous Sequential Circuits: Mealy vs. Moore FSMs ..... 1
Finite State Machine Design Workflow ..... 1
3.6 High-Yield University Exam Question Bank & Model Answers ..... 1
Part A: Short Answer Questions (2–3 Marks) ..... 1
Part B: Long Answer Questions (8–10 Marks) ..... 1
3.7 Unit III Summary & Quick Revision Sheet ..... 1

# 3.1 Flip-Flops: Types, Truth Tables & Excitation Tables

**Definition: Sequential Circuit vs. Combinational Circuit**

*In a Combinational Circuit, output depends strictly on present inputs. In a Sequential Circuit, output depends on both Present Inputs and Past State History stored in internal Memory Elements (Latches / Flip-Flops).*

| Flip-Flop Type | Characteristic Equation Q_(n+1) | Excitation Table: Q_n → Q_(n+1) [0→0, 0→1, 1→0, 1→1] | Key Operational Behavior |
|---|---|---|---|
| SR Flip-Flop | Q_(n+1) = S + R' Q_n (Constraint: S • R = 0) | S: [0, 1, 0, ×], R: [×, 0, 1, 0] | S=R=1 is Invalid / Forbidden State in basic latch. |
| JK Flip-Flop | Q_(n+1) = J Q_n' + K' Q_n | J: [0, 1, ×, ×], K: [×, ×, 1, 0] | J=K=1 toggles output. Overcomes SR invalid state. |
| D Flip-Flop | Q_(n+1) = D | D: [0, 1, 0, 1] | Data / Transparent latch; output follows D on active clock edge. |
| T Flip-Flop | Q_(n+1) = T ⊕ Q_n = T Q_n' + T' Q_n | T: [0, 1, 1, 0] | Toggle Flip-Flop (T=1 toggles, T=0 holds state). Used in counters. |

## Race-Around Condition & Master-Slave JK Flip-Flop

**The Race-Around Condition in Level-Triggered JK Flip-Flops**

*When J=K=1 and clock pulse width t_p is greater than the propagation delay t_pd of the flip-flop (t_p > t_pd), the output toggles repeatedly and unpredictably back and forth between 0 and 1 during a single clock pulse, producing an undefined output state.*

• *Solution (Master-Slave JK Flip-Flop): Uses two JK flip-flops in series. Master is enabled on Clock=1 (samples inputs); Slave is enabled on Clock=0 (inverter transfers master state to outputs). Output toggles exactly ONCE per clock cycle!*

# 3.2 Systematic Flip-Flop Conversion Methodology

To convert an Available Flip-Flop (e.g., JK) into a Required Target Flip-Flop (e.g., D or T):

- **Step 1:** Construct the Characteristic Table for the Required Target Flip-Flop listing Inputs, Present State Q_n, and Next State Q_(n+1).
- **Step 2:** Using the Excitation Table of the Available Flip-Flop, fill in the required excitation inputs (e.g., J and K) for each state transition (Q_n → Q_(n+1)).
- **Step 3:** Plot K-maps for each input of the available flip-flop in terms of the target inputs and Q_n, and derive minimal Boolean equations.
- **Step 4:** Draw the final logic diagram connecting external gating to the available flip-flop.

# 3.3 Shift Registers & Shift Register Counters

## 1. Shift Register Configurations

- • **SISO (Serial-In, Serial-Out):** Data enters one bit per clock cycle and exits one bit per cycle. n clock cycles to load, n clock cycles to retrieve.
- • **SIPO (Serial-In, Parallel-Out):** Data loaded serially in n cycles; all n bits available simultaneously on parallel output pins.
- • **PISO (Parallel-In, Serial-Out):** Data loaded simultaneously in 1 cycle using Shift/Load control line; shifted out serially.
- • **PIPO (Parallel-In, Parallel-Out):** Data loaded and retrieved in a single clock cycle (High-speed buffer register).
- • **4-Bit Universal Shift Register (IC 74194):** Operates in 4 modes via Select lines S_1, S_0: [00: Hold state, 01: Shift Right, 10: Shift Left, 11: Parallel Load].

## 2. Ring Counter vs. Johnson Counter

| Feature / Parameter | Ring Counter (Mod-N) | Johnson / Twisted-Ring Counter (Mod-2N) |
|---|---|---|
| Feedback Connection | Output of last stage (Q_n-1) is fed directly back to first stage input (D_0 = Q_n-1). | Inverted output of last stage (Q'_n-1) is fed back to first stage input (D_0 = Q'_n-1). |
| Number of Unique States | Modulus = N states (e.g., 4 flip-flops produce 4 states: 1000 → 0100 → 0010 → 0001). | Modulus = 2N states (e.g., 4 flip-flops produce 8 states: 0000 → 1000 → 1100 → 1110 → 1111 → 0111 → 0011 → 0001). |
| Decoding Complexity | Self-decoding; each state directly identified by a single high output bit without logic gates. | Requires simple 2-input AND gates to decode each of the 2N states. |

| Feature / Parameter | Ring Counter (Mod-N) | Johnson / Twisted-Ring Counter (Mod-2N) |
|---|---|---|
| Unused States & Lockout | (2^N - N) unused states. Requires self-starting gating to prevent lockout in invalid loops. | (2^N - 2N) unused states. Requires self-starting feedback gating. |

# 3.4 Counters: Asynchronous, Synchronous & IC 7490

## Asynchronous (Ripple) vs. Synchronous Counters

| Comparison Criteria | Asynchronous (Ripple) Counter | Synchronous Counter |
|---|---|---|
| Clock Signal Connection | Clock pulses applied ONLY to the first (LSB) flip-flop. Subsequent flip-flops are clocked by output (Q or Q') of preceding stage. | Clock pulses applied SIMULTaneously to the clock inputs of ALL flip-flops. |
| Operating Speed & Delay | Slow; total propagation delay accumulates through all n stages (Delay = n × t_pd). Maximum frequency limited. | High-speed; total delay equals propagation delay of single flip-flop plus gating delay (Delay = t_pd + t_gate). |
| Glitches / Decoding Spikes | Prone to severe output glitches due to unequal propagation delays between bits. | Glitch-free; all outputs change state at the exact same instant. |
| Design Complexity | Extremely simple circuit wiring. | Requires additional combinational excitation gating (AND gates) to determine toggle conditions. |

## The IC 7490 BCD Decade Counter

**IC 7490 Internal Architecture**

*IC 7490 is a monolithic decade counter containing an internal MOD-2 counter (Section A) and a MOD-5 counter (Section B):*

- *MOD-10 (BCD Counter Configuration): Connect external clock to Clock A (pin 14), and externally connect Q_A output (pin 12) to Clock B input (pin 1). Provides standard BCD 0-9 count.*
- *MOD-6 Counter (Digital Clocks): Connect Q_B and Q_C to asynchronous reset pins R_0(1) and R_0(2) to reset upon reaching state 6 (0110_2).*

# 3.5 Synchronous Sequential Circuits: Mealy vs. Moore FSMs

| FSM Architecture | Output Dependency Rule | State Diagram Representation | Timing & Hardware Characteristics |
|---|---|---|---|
| Moore Machine | Outputs depend SOLELY on the Present State of the system: Z = λ(S_present). | Outputs are written inside the state circle: [State / Output]. | Outputs are synchronous with clock; immune to input glitch transitions; requires more states. |
| Mealy Machine | Outputs depend on BOTH Present State AND Present Inputs: Z = λ(S_present, X_in). | Outputs are written on the state transition arrows: [Input / Output]. | Outputs react immediately to asynchronous input changes; fewer states needed, but can produce glitches. |

### Finite State Machine Design Workflow

- **1. State Diagram & State Table:** Map verbal specifications into formal state transitions.
- **2. State Reduction:** Eliminate redundant equivalent states using Row Matching (identical next-states and outputs) or the Implication Table Method.
- **3. State Assignment:** Assign unique binary codes to symbolic states (e.g., Gray code or One-Hot encoding).
- **4. Flip-Flop Excitation & Gate Synthesis:** Derive flip-flop input equations via K-maps and draw logic diagram.

## 3.6 High-Yield University Exam Question Bank & Model Answers

### Part A: Short Answer Questions (2–3 Marks)

- **Q1. What is the Race-Around Condition in JK Flip-Flops? How is it resolved?**

Answer: The Race-Around condition occurs in level-triggered JK flip-flops when J=K=1 and clock pulse width t_p > t_pd (propagation delay), causing the output to toggle uncontrollably during the clock high period. It is eliminated by using Edge-Triggering or Master-Slave JK Flip-Flop architecture.

- **Q2. Differentiate between Mealy and Moore state machines.**

Answer: In a Moore machine, output depends strictly on the present state. In a Mealy machine, output depends on both the present state and the current input, allowing Mealy machines to typically require fewer states.

- **Q3. Compare a 4-bit Ring Counter and a 4-bit Johnson Counter.**

Answer: A 4-bit Ring Counter connects Q_3 → D_0, producing N = 4 unique states (self-decoding). A 4-bit Johnson Counter connects Q'_3 → D_0, producing 2N = 8 unique states (double the state capacity).

- **Q4. How is IC 7490 configured as a MOD-10 BCD counter?**

Answer: Connect the input clock signal to Clock A (pin 14), and externally connect the output Q_A (pin 12) of the internal MOD-2 counter to the input Clock B (pin 1) of the internal MOD-5 counter.

### Part B: Long Answer Questions (8–10 Marks)

- **Q5. Design a Synchronous 3-Bit Up/Down Counter using JK Flip-Flops. Include the state diagram, excitation table, K-map simplifications, and complete logic circuit diagram.**

Model Answer Outline:

- 1. State diagram: 8 states (000 to 111) controlled by mode line M (M=0 for UP count, M=1 for DOWN count).
- 2. State table and excitation table mapping Q_2, Q_1, Q_0 transitions to J_2, K_2, J_1, K_1, J_0, K_0.
- 3. K-map simplifications:
- - J_0 = K_0 = 1.
- - J_1 = K_1 = M' Q_0 + M Q_0'.
- - J_2 = K_2 = M' Q_1 Q_0 + M Q_1' Q_0'.
- 4. Complete logic circuit schematic with 3 JK flip-flops, common clock line, and control gating.

- **Q6. Convert a JK Flip-Flop into a D Flip-Flop and a T Flip-Flop. Show complete step-by-step conversion tables, K-maps, and final logic schematics.**

Model Answer Outline:

- 1. JK to D Conversion: Construct D characteristic table → Map Q_n, Q_(n+1) to JK excitation table → K-maps derive J = D and K = D' → Draw JK flip-flop with inverter on K input.
- 2. JK to T Conversion: Construct T characteristic table → Map to JK excitation table → K-maps derive J = T and K = T → Draw JK flip-flop with J and K tied together to input T.
- 3. Verification proof verifying that truth tables match target specifications.

## 3.7 Unit III Summary & Quick Revision Sheet

| Sequential Topic | Key Theoretical & Design Takeaways for Exams |
|---|---|
| Flip-Flops | SR (S•R=0), JK (J=K=1 toggles, race-around solved by Master-Slave), D (Data Q_(n+1)=D), T (Toggle Q_(n+1)=T⊕Q). |
| Shift Registers | SISO, SIPO, PISO, PIPO. Universal 74194 (Hold, Shift R, Shift L, Parallel Load). |
| Ring & Johnson | Ring (Q_last → D_0, N states), Johnson (Q'_last → D_0, 2N states). |

| Sequential Topic | Key Theoretical & Design Takeaways for Exams |
|---|---|
| Counters & 7490 | Ripple (Async, delay accumulates) vs Synchronous (Common clock). 7490: MOD-2 + MOD-5 → MOD-10. |
| FSM (Mealy vs Moore) | Moore (Output = f(State)), Mealy (Output = f(State, Input)). State reduction via Implication table. |